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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,845	07/10/2003	Daniel M. Dreps	AUS920030015US1	1731

7590 12/20/2004

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EXAMINER	
TAN, VIBOL	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 12/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,845	DREPS ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 9 and 10 are objected to because of the following informalities: the negative input of receiver/comparator 204 shown coupling to Vref in Fig. 2, whereas the claims recite coupling to the threshold voltage. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 5-7 and 26-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 5, it is not so clear how the first termination network that is coupled to the common node in response to the fifth and sixth signals generated by logic circuitry (as recitation of claim 4) is also in response to a first logic state of the first control signal and a first logic state of the second control signal, as recited in claim 5. Clarification is necessary.

Claim 26 rejected in the same manner as claim 5.

In claim 7, it is not so clear how the third termination network that is coupled to the common node in response to the third and fourth signals generated by logic circuitry (as recitation of claim 3) is also in response to a first logic state of the fifth control signal and a first logic state of the sixth control signal, as recited in claim 5. Clarification is necessary.

Claim 28 rejected in the same manner as claim 7.

Claim 6 recites the limitation "said third control signal... and said fourth control signal" in lines 3 and 8, respectively. There is insufficient antecedent basis for this limitation in the claim.

Claim 27 rejected in the same manner as claim 6.

4. Claims 12-16 and 33-36 recite the limitation "TL". There is insufficient antecedent basis for this limitation in the claim. If "TL" stands for transmission line, then TL should be in parenthesis in the previous claim(s).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-4 and 8-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (U. S. PAT. 6,556,038).

In claim 1, Kim et al. teaches all claimed features in Figs. 5-10, a receiver circuit for terminating a transmission line comprising: a receiver (20) having an input (not marked) coupled to a transmission line output (pad 100 or 200) of said transmission line (Zo) forming a common node (a node connecting the output of the transmission line and the input of the receiver, pad), an output generating a digital signal (output from 20) in

response to a signal (signal at pad 100 or 200) at said transmission line output and a threshold voltage (a turning on voltage of 20); a termination network (30) coupled to said common node for setting a plurality of Thevenins voltages (31, 33) and Thevenins impedances (resistance of 31 and 33) in response to a plurality of control signals (NA0-NA4 and NB0-NB4); and logic circuitry (PIUC & PIDC) for generating said plurality of control signals in response to a plurality of mode setting inputs (input signals provided to PIUC & PIDC).

In claim 2, Kim et al. teaches all claimed features in Figs. 5-10, a receiver circuit for terminating a transmission line comprising: a receiver (20) having an input (not marked) coupled to a transmission line output (pad 100 or 200) of said transmission line (Zo) forming a common node (a node connecting the output of the transmission line and the input of the receiver, pad), an output generating a digital signal (output from 20) in response to a signal (signal at pad 100 or 200) at said transmission line output and a threshold voltage (a voltage from 30); a termination network (30) coupled to said common node for setting a plurality of Thevenins voltages (31, 33) and Thevenins impedances (resistance of 31 and 33) in response to a plurality of control signals (NA0-NA4 and NB0-NB4); and logic circuitry (PIUC & PIDC) for generating said plurality of control signals in response to a plurality of mode setting inputs (input signals provided to PIUC & PIDC); wherein said termination network comprises: a first termination network (a first pull-up transistor and a first pull-down transistor) coupled to said common node and setting a Thevenins impedance and a Thevenins voltage at said common node; and a second termination network (a second pull-up transistor and a second pull-down

transistor) coupled to said common node (pad) and modifying said Thevenins impedance and said Thevenins voltage in response to first and second control signals (NA1, NB1).

In claim 3, Kim et al. further teaches the circuit of claim 2 further comprising a third termination network (a third pull-up transistor and a third pull-down transistor) coupled to said common node (pad) and modifying said Thevenins impedance and said Thevenins voltage in response to third and fourth control signals (NA2, NB2) generated by said logic circuitry (PIUC & PIDC).

In claim 4, Kim et al. further teaches the circuit of claim 2, wherein said first termination network (a first pull-up transistor and a first pull-down transistor) is coupled to said common node (pad) in response to fifth and sixth control signals (NA0, NB0) generated by said logic circuitry.

In claims 8 and 9, Kim et al. further teaches the circuit of claim 2, wherein said receiver circuit is a logic gate (receiver 20 is a logic gate) having a first logic input (positive input terminal) coupled to said receiver input (coupled to pad 100 or 200), a second logic input (negative input terminal) coupled to a voltage (Vref) corresponding to a first logic state, wherein said threshold voltage is a switching voltage (a voltage required to turn on any transistor inside a logic gate) of said logic gate and is generated internal to said logic gate (20); and wherein said receiver circuit is a comparator (as shown in Fig. 7) having a positive input coupled to said input of said receiver, a negative input coupled to said threshold voltage (Vref in this case) and a comparator output coupled to said receiver output (comparator output is same as receiver output from 20).

In claim 10, Kim et al. further teaches the circuit of claim 4, wherein said receiver circuit is a comparator (col. 7, line 63) having a positive input coupled to said input of said receiver, a negative input coupled to said threshold voltage (Vref in this case) and a comparator output coupled to said receiver output.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 5-7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. in view of Barraclough (U. S. PAT. 5,739,707).

In claim 5, Kim et al. teaches all claimed features the circuit of claim 4; with the exception of teaching wherein said first termination network comprises: a first resistor having a first terminal coupled to a first power supply voltage with a first electronic switch; a second resistor having a first terminal coupled to said second terminal of said first resistor and said common node and a second terminal coupled to a second power supply voltage with a second electronic switch. However, Barraclough teaches in Fig. 4, a first resistor (411) having a first terminal coupled to a first power supply voltage (VDD) with a first electronic switch (401; a second resistor (416) having a first terminal coupled to said second terminal (425) of said first resistor and said common node (425 is a common node) and a second terminal coupled to a second power supply voltage (VSS) with a second electronic switch (406).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to place resistors, as taught by Barraclough, into the circuit of Kim et al. to provide a receiver circuit having a constant impedance voltage source with slew rate limiting.

Claims 6 and 7 are rejected basically in the same manner with regard to claim 5.

In claim 11, Kim et al. in view of Barraclough teaches the claimed features of claim 7; with the exception of teaching wherein the threshold voltage is equal to one half the difference between said first and second power supply voltages. However, it would have been obvious to one ordinary skill in the art the time of the invention was made to select the threshold voltage is equal to one half the difference between said first and second power supplies (in this case one half of VDDQ), since it has been held that where the general conditions of the claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

9. Claims 22-25 and 25-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muljono (U. S. PAT. 6,347,350) in view of Kim et al.

In claim 22, Muljono teaches claimed features in Fig. 7, an integrated circuit (IC) comprising: a digital processor (702); memory (704 or 706) for storing instructions and data for said processor; input/output (I/O) interface circuitry (708 or 710) for communicating to device circuitry external (other device) to said IC; a receiver circuit (col. 7, line 18) in said interface circuitry for terminating a transmission line (712) coupling said receiver circuit to said device circuitry; and Kim et al. teaches in Figs. 5-

10, wherein the receiver (20) having an input (not marked) coupled to a transmission line output (pad 100 or 200) of said transmission line (Zo) forming a common node (a node connecting the output of the transmission line and the input of the receiver, pad), an output generating a digital signal (output from 20) in response to a signal (signal at pad 100 or 200) at said transmission line output and a threshold voltage (a turning on voltage of 20); a termination network (30) coupled to said common node for setting a plurality of Thevenins voltages (31, 33) and Thevenins impedances (resistance of 31 and 33) in response to a plurality of control signals (NA0-NA4 and NB0-NB4); and logic circuitry (PIUC & PIDC) for generating said plurality of control signals in response to a plurality of mode setting inputs (input signals provided to PIUC & PIDC).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Muljono and the teachings of Kim et al. in order to provide a computer system having a terminator circuit for receiving and terminating an external input signal.

In claim 23, Muljono teaches claimed features in Fig. 7, an integrated circuit (IC) comprising: a digital processor (702); memory (704 or 706) for storing instructions and data for said processor; input/output (I/O) interface circuitry (708 or 710) for communicating to device circuitry external (other device) to said IC; a receiver circuit (col. 7, line 18) in said interface circuitry for terminating a transmission line (712) coupling said receiver circuit to said device circuitry; and Kim et al. teaches in Figs. 5-10, wherein the receiver (20) having an input (not marked) coupled to a transmission line output (pad 100 or 200) of said transmission line (Zo) forming a common node (a

node connecting the output of the transmission line and the input of the receiver, pad), an output generating a digital signal (output from 20) in response to a signal (signal at pad 100 or 200) at said transmission line output and a threshold voltage (a turning on voltage of 20); a termination network (30) coupled to said common node for setting a plurality of Thevenins voltages (31, 33) and Thevenins impedances (resistance of 31 and 33) in response to a plurality of control signals (NA0-NA4 and NB0-NB4); and logic circuitry (PIUC & PIDC) for generating said plurality of control signals in response to a plurality of mode setting inputs (input signals provided to PIUC & PIDC); wherein said termination network comprises: a first termination network (a first pull-up transistor and a first pull-down transistor) coupled to said common node and setting a Thevenins impedance and a Thevenins voltage at said common node; and a second termination network (a second pull-up transistor and a second pull-down transistor) coupled to said common node (pad) and modifying said Thevenins impedance and said Thevenins voltage in response to first and second control signals (NA1, NB1).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Muljono and the teachings of Kim et al. in order to provide a computer system having a terminator circuit for receiving and terminating an external input signal.

In claim 24, Kim et al. further teaches the circuit of claim 23 further comprising a third termination network (a third pull-up transistor and a third pull-down transistor) coupled to said common node (pad) and modifying said Thevenins impedance and said

Thevenins voltage in response to third and fourth control signals (NA2, NB2) generated by said logic circuitry (PIUC & PIDC).

In claim 25, Kim et al. further teaches the circuit of claim 23, wherein said first termination network (a first pull-up transistor and a first pull-down transistor) is coupled to said common node (pad) in response to fifth and sixth control signals (NA0, NB0) generated by said logic circuitry.

In claims 29 and 30, Kim et al. further teaches the circuit of claim 23, wherein said receiver circuit is a logic gate (receiver 20 is a logic gate) having a first logic input (positive input terminal) coupled to said receiver input (coupled to pad 100 or 200), a second logic input (negative input terminal) coupled to a voltage (Vref) corresponding to a first logic state, wherein said threshold voltage is a switching voltage (a voltage required to turn on any transistor inside a logic gate) of said logic gate and is generated internal to said logic gate (20); and wherein said receiver circuit is a comparator (as shown in Fig. 7) having a positive input coupled to said input of said receiver, a negative input coupled to said threshold voltage (Vref in this case) and a comparator output coupled to said receiver output (comparator output is same as receiver output from 20).

In claim 31, Kim et al. further teaches the circuit of claim 25, wherein said receiver circuit is a comparator (col. 7, line 63) having a positive input coupled to said input of said receiver, a negative input coupled to said threshold voltage (Vref in this case) and a comparator output coupled to said receiver output.

10. Claims 26-28 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muljono in view of Kim et al. as applied to claim 22 above, and further in view of Barraclough.

In claim 26, Muljono in view of Kim et al. teaches all claimed features, the IC of claim 22, as explained above; with the exception of teaching in detail of the termination network comprises first and second resistors. However, Barraclough teaches in Fig. 4, a first resistor (411) having a first terminal coupled to a first power supply voltage (VDD) with a first electronic switch (401; a second resistor (416) having a first terminal coupled to said second terminal (425) of said first resistor and said common node (425 is a common node) and a second terminal coupled to a second power supply voltage (VSS) with a second electronic switch (406).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to place resistors, as taught by Barraclough, into the circuit of Kim et al. to provide a receiver circuit having a constant impedance voltage source with slew rate limiting.

Claims 27 and 28 are rejected basically in the same manner with regard to claim 26.

In claim 32, Muljono in view of Kim et al. and further in view of Barraclough teaches the claimed features of claim 28; with the exception of teaching wherein the threshold voltage is equal to one half the difference between said first and second power supply voltages. However, it would have been obvious to one ordinary skill in the art the time of the invention was made to select the threshold voltage is equal to one

half the difference between said first and second power supplies (in this case one half of VDDQ), since it has been held that where the general conditions of the claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

11. Claims 17-21 and 38-42 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

12. Applicant's arguments with respect to claims 1 and 22 have been considered but are moot in view of the new ground(s) of rejection.

Further consideration results in new ground of rejections, as explained in details above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vibol Tan

Primary Examiner, AU 2819

VIBOL TAN
PRIMARY EXAMINER